12.6 A CMOS 1Gb/s 5-Tap Transversal Equalizer Based on Inductorless 3rd-Order Delay Cells

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To compensate for the frequency-dependent loss in backplane and wireline communications, analog transversal equalizers have been used successfully in gigabit receivers. One of the main challenges in the design of high-speed transversal equalizers is the implementation of the delay cells, denoted as z^{-1} in Fig. 12.6.1. Sampled-data architectures [1] are limited in speed due to the large time constants associated with the charge/discharge of sampling capacitors. Although parallelism improves speed, complexity and silicon area increase while requiring large power consumption [2]. Ideally, delay cells must implement a transfer function given by $H(\omega)=e^{-j\omega T_d}$, where T_d is the desired delay. They should provide a constant group delay and magnitude response over the bandwidth of the data, which in the case of NRZ binary signals is approximately half the data rate (500MHz for 1Gb/s). Emulation of transmission lines [3] using on-chip inductors is impractical for data rates <10Gb/s due to the size of inductors. First-order Pade delay lines proposed in [4] have large group delay variations. For example, a 500ps delay line with this approach would have 200ps variation (40%) within a 500MHz bandwidth.

To achieve constant group delay, linear-phase filter approximations such as Bessel maximally flat delay and linear-phase with equiripple phase error of 0.05° can be used. For a T/2 fractionally-spaced equalizer at 1Gb/s, a delay of 500ps is required for each cell. The group delay versus frequency of linear-phase with equiripple phase error of 0.05° approximations (normalized to a delay of 500ps) is shown in Fig. 12.6.2 for various filter orders (N). The resulting 3dB bandwidth is shown in the same figure. For a constant group delay and flat magnitude response over >500MHz, at least a 3rd-order cell is required; a 2nd-order cell such as the one reported in [5] tuned for 500ps delay would not provide the required bandwidth.

The proposed 3rd-order delay cell to implement each z^{-1} block is depicted in Fig. 12.6.3. Derived from the LC ladder prototype shown in the same figure, the OTA-C realization incorporates active inductor emulation ($L_2 = C_2/(g_{m1}g_{m3})$) as well as active terminations ($R_{S,L} = 1/g_{m2}$) at ports A and B that are implemented by using NMOS loads (transistors M_2 in Fig. 12.6.3) at the output of 2 of the amplifiers in the inductive emulation. The operating point at the input and output ports is fixed by the delay cell terminations (M_2); hence only one common-mode feedback (CMFB) circuit is required for the entire structure. The low-Q of the complex poles required in the filter prototype (Q=0.8) is exploited and simple single-stage low-gain (26dB) OTAs are used for g_{m3} in the inductive emulation without the need of long-channel output devices that would otherwise increase the parasitic capacitances. Similarly, g_{m0} is a single-stage OTA that does not require a large gain since it is connected to a low-impedance at port A. These features lead to a compact low-power realization of the 3rd-order delay cell. Current I_{bias1} controls the gain while I_{bias2} sets the group delay, providing a tuning range from 420ps to 590ps with <10% ripple within 500MHz. Simulations over process corners and temperatures of -20°C to 100°C show variations in the low-frequency group delay within 15%. Designed in a standard 0.35µm CMOS process, the delay cell consumes 16.8mW (Supply = ±1.5V) when tuned for a nominal delay of 500ps at 27°C room temperature.

The parasitic capacitance imposed by the multipliers, typically Gilbert cells as shown in Fig. 12.6.4, or variable gain amplifiers, limits the frequency response of the summing node (the node at which the output currents of the multipliers are tied together and summed). To convert the sum of currents into an output voltage, a resistive load is commonly used [5]. The frequency of the parasitic pole at this node leads to a trade-off between gain and bandwidth. A 5-tap equalizer in 0.35µm CMOS using Gilbert cells as multipliers, driving a resistive load of R_L = 1kΩ results in a bandwidth of 275MHz, certainly not enough for a 1Gb/s equalizer. To increase the frequency of the pole at the summing node without degrading the gain, cascode devices can be used to introduce a low resistance at this node, as previously reported in [1]. Nevertheless, the frequency of the pole at the output node is still limited.

To further improve the bandwidth of the summing circuit and I/V converter, a transimpedance load is proposed, as shown in Fig. 12.6.4. The load, composed of a TIA implemented by M_3 and R_1, leads to a transimpedance gain of $T_{Gain} = -R_1$, assuming $R_2 >> R_1 >> 1/g_{m3}$ (g_{m3} denoting the transconductance of M_3). Resistors R_2 bias the gates of M_4, and M_5 (which provides the bias current for the Gilbert cells) to avoid the use of additional CMFB circuits, therefore reducing power consumption. The circuit effectively introduces a low resistance at both, the summing and the output nodes, leading to 2 high-frequency poles approximately given by $\omega_1 = g_{m3}/(C_p + C_{gs,3})$ and $\omega_2 = g_{m3}/C_L$, where C_p is the total parasitic capacitance of the 5 multipliers, $C_{gs,3}$ is the parasitic capacitance added by M_3, and C_L is the load capacitance due to the next stage, typically a limiting amplifier. This circuit provides a wider bandwidth compared to the resistive and cascode approaches even with the additional capacitance $C_{gs,3}$ (~200fF). Using this technique, the 3dB bandwidth of the summing circuit is increased to 1GHz (R_L = 1kΩ, g_{m3} = 7mA/V), while the cascode approach leads to a bandwidth of only 520MHz, which would result in larger deterministic jitter. The total power consumption of the 5 multipliers (Gilbert cells) is 22.5mW; the TIA consumes an additional 6mW.

The transversal equalizer was fabricated in a 0.35µm CMOS process (f_t ~ 15GHz). The measured group delay of a stand-alone delay cell is presented in Fig. 12.6.5, showing variations of <40ps within a 500MHz bandwidth. The measured IM_3 of the delay cell for a 300mV$_{pp}$ input is -27dB.

The equalizer is used to compensate for the frequency-dependent loss in CAT5e twisted-pair cable. The measured attenuation of a 15m cable at 500MHz is 8dB, and 13dB for a length of 23m. The eye-pattern diagrams with a 1Gb/s PRBS of length 2^{23}-1 are shown in Fig. 12.6.6. For 15m, the vertical eye opening before and after equalization are 15% and 59%, respectively. For 23m, the vertical eye opening before and after equalization are 0% and 58%, respectively. The chip micrograph is shown in Fig. 12.6.7 (die size is 1.8×1.8mm^2). The total power dissipation of the equalizer is 96mW from a ±1.5V supply and occupies 0.26mm^2. While proper operation is demonstrated at 1Gb/s in 0.35µm, the proposed 3rd-order delay cells and broadband summing circuit are estimated to enable the design of low-power inductorless T/2 transversal equalizers at speeds above 7Gb/s in a 0.13µm CMOS process.

Acknowledgements:
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References:
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[2] J. E. Jaussi, G. Balamurugan, D. R. Johnson, et al., "8-Gb/s Source-Synchronous I/O Link with Adaptive Receiver Equalization, Offset Cancellation, and Clock De-skew," *IEEE J. Solid-State Circuits,* vol. 40, pp. 80-88, Jan., 2005.
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[4] J. Buckwalter and A. Hajimiri, "An Active Analog Delay and the Delay Reference Loop," *RFIC Symp. Dig. Papers,* pp. 17-20, Jun., 2004.
[5] X. Lin, S. Saw, and J. Liu, "A CMOS 0.25-µm Continuous-Time FIR Filter with 125 ps per Tap Delay as a Fractionally Spaced Receiver Equalizer for 1-Gb/s Data Transmission," *IEEE J. Solid-State Circuits,* vol. 40, pp. 593-602, Mar., 2005.

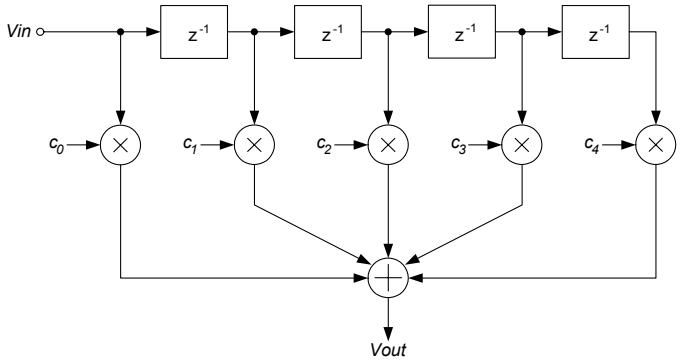


Figure 12.6.1: 5-tap transversal equalizer structure.

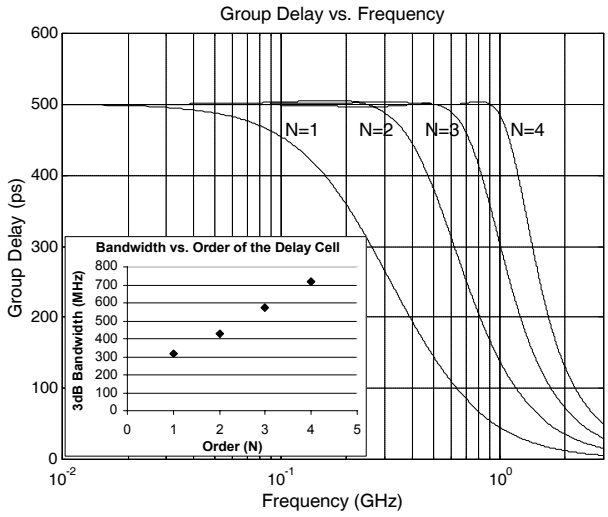
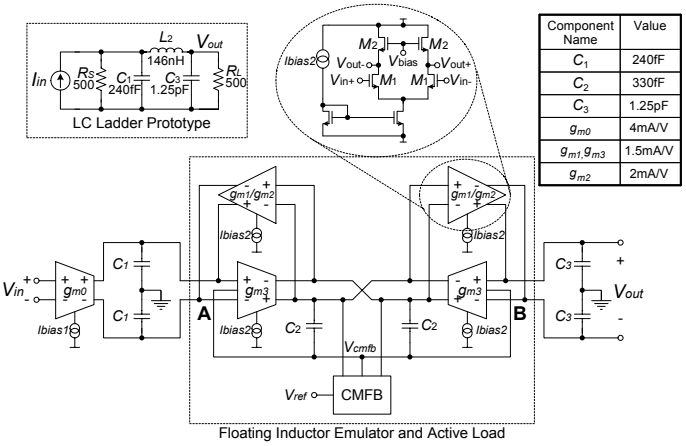


Figure 12.6.2: Group delay versus frequency and resulting 3dB bandwidth.



Component Name	Value
C_1	240fF
C_2	330fF
C_3	1.25pF
g_{m0}	4mA/V
g_{m1}, g_{m3}	1.5mA/V
g_{m2}	2mA/V

Figure 12.6.3: 3rd-order delay cell.

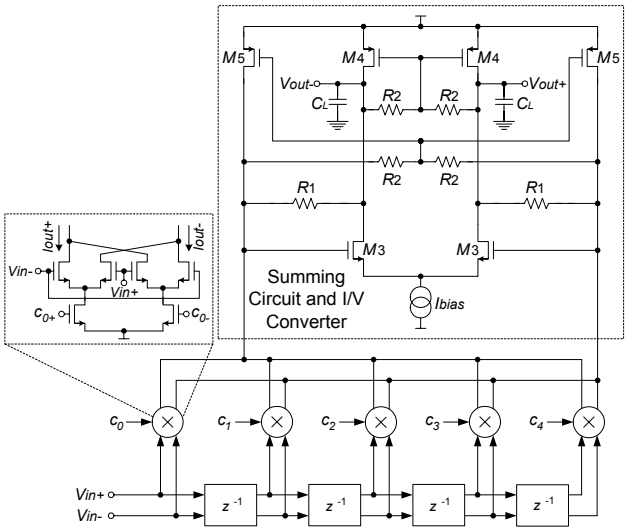


Figure 12.6.4: Summing circuit and I/V converter.

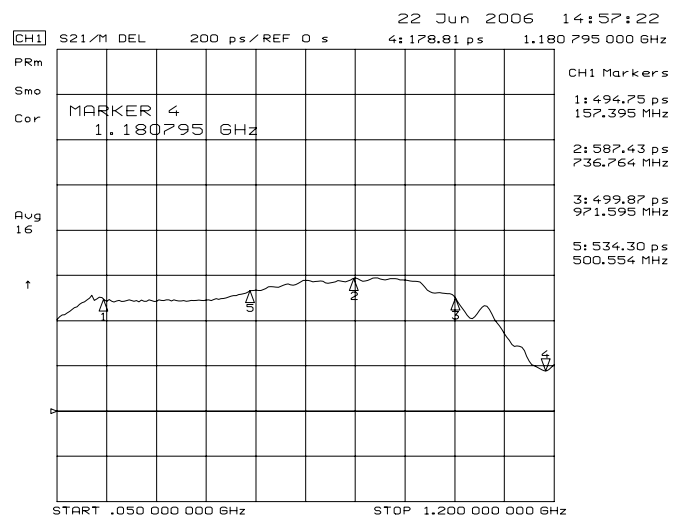


Figure 12.6.5: Measured group delay of 3rd-order delay cells.

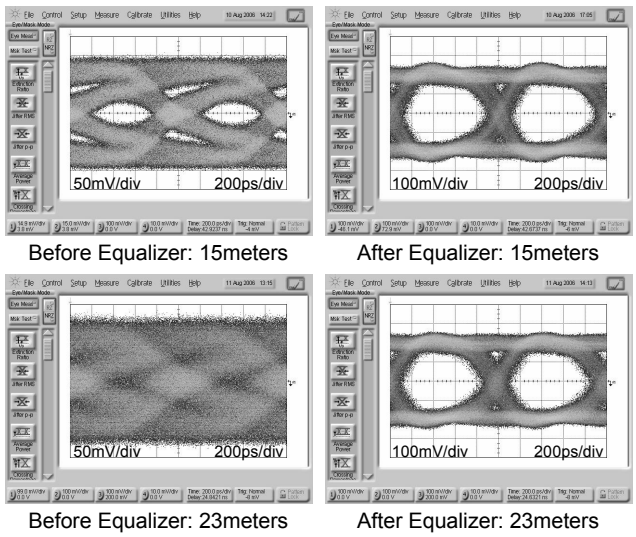


Figure 12.6.6: Measured eye-pattern diagrams.

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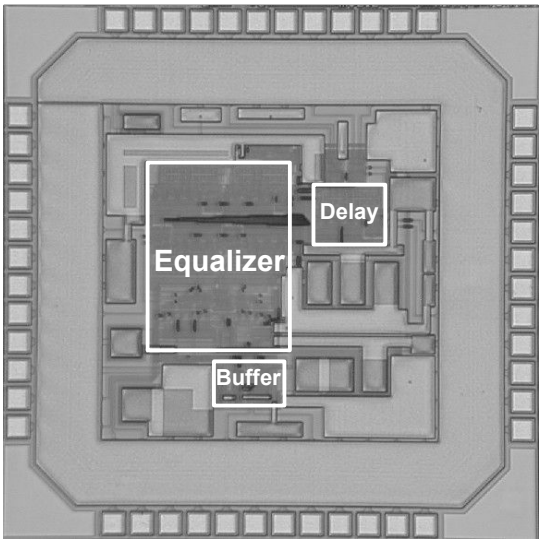

Figure 12.6.7: Chip micrograph.

